



VISVESVARAYA

COLLEGE OF ENGINEERING & TECHNOLOGY



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2.3.1 Student centric methods, such as experiential learning, participative learning and problem-solving methodologies are used for enhancing learning experiences

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S. No	Description
1	Sample copy of Laboratory Sessions
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17	Sample copy of Virtual labs


Principal

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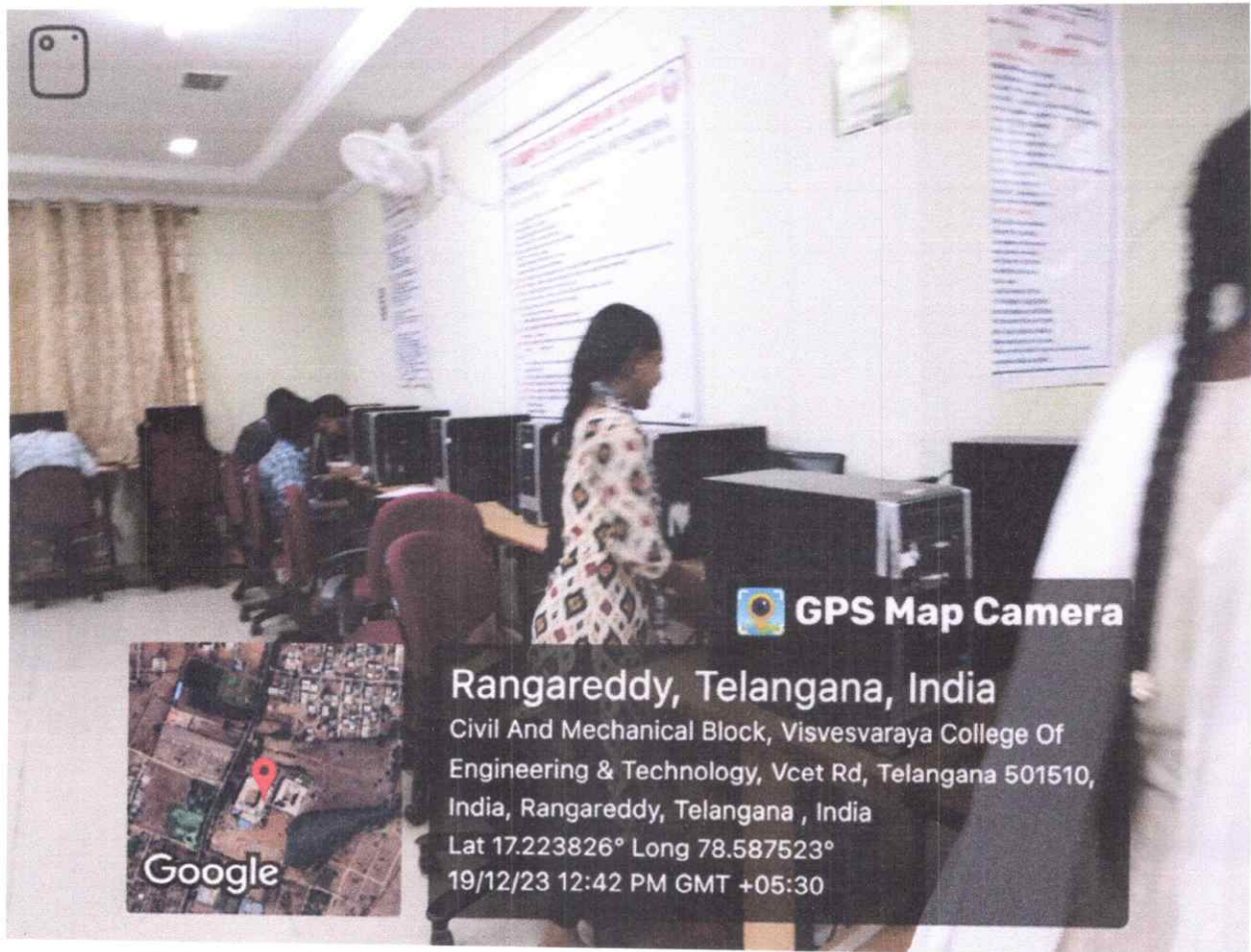
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Experiential Learning: The institution offers experiential learning for students with the following approaches:

1.Laboratory Sessions: Laboratory sessions are conducted for better understanding of theoretical concepts



Students of CSE Department, III Year I Semester performing Lab Experiments in "COMPLIER DESIGN LAB"(A.Y 23-24)

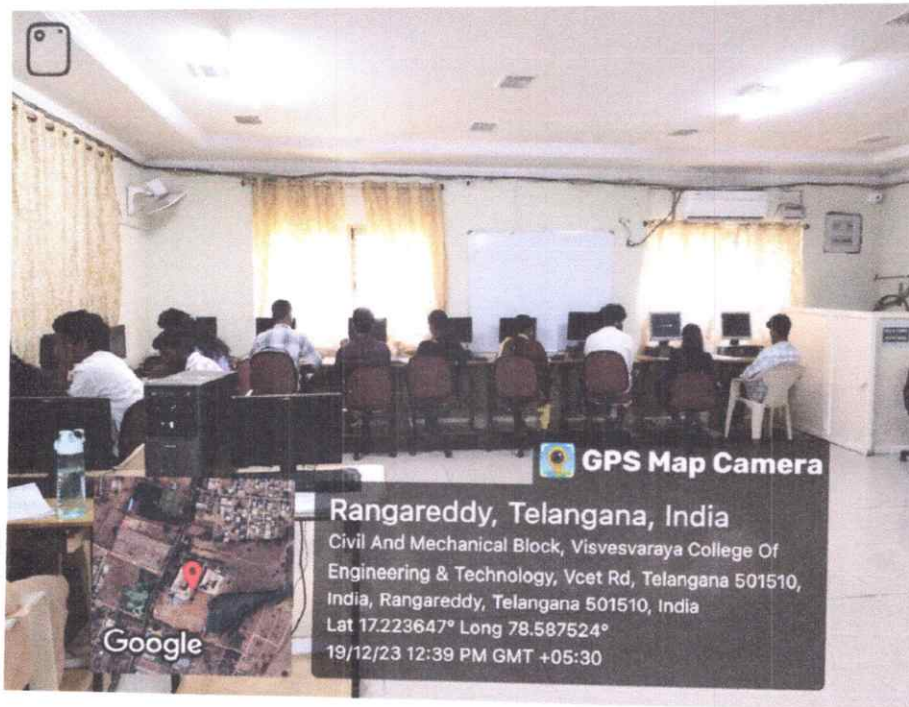
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Students of CSE Department,II Year I Semester performing Lab Experiments in “DATABASE MANAGEMENT LAB”(A.Y 23-24)



Students of CSE Department,III Year I Semester performing Lab Experiments in “SOFTWARE TESTING LAB”(A.Y 23-24)



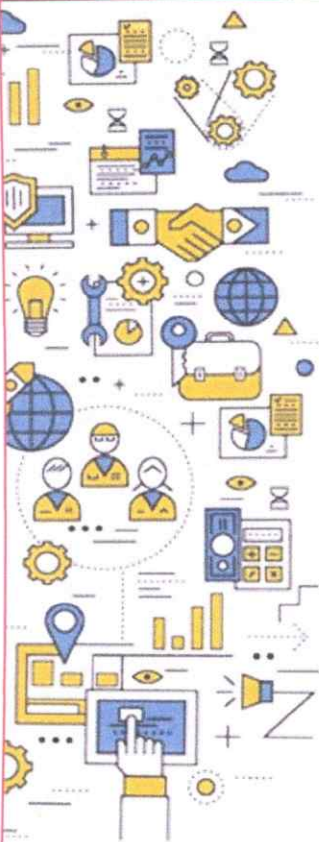
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2. INTERNSHIPS: Internships are provided to the students.






Building a better
workforce

EY CERTIFICATE






INTERNSHIP_1706828655860db357f2

OF APPRECIATION


PROUDLY PRESENTED TO

I KARTHIK REDDY
STU657a90855967f1702531205

for successfully completing the 6th EY Global Delivery Services led weeks of internship in collaboration 28 February 2024 to 25 April 2024 with AICTE from Full Stack Web on Next Gen Employability Program Development under the 2023-24.



Nagesh Singh
Executive Director
Edunet Foundation



Dr. Ramesh Unnikrishnan
Advisor-II,
AICTE

Mr. I. KARTHIK REDDY, student of CSE Department has completed internship at EY(A.Y 2023-24)


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3. Industrial study visits & Field visits: Organized to expose to current technologies and to provide an opportunity to learn practically through interaction through interaction



Industrial study visits to National Academy of Construction in 2022

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4. Industry driven competition:

Students encouraged participating in competition to show their creative ideation and talent



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*Management, Principal & Faculty of
Visvesvaraya college of Engg and Technology
Congratulate IV year Mechanical Engg students,
A.SATHISH(19BT5A0301)*

R.RAJITHA(19BT5A0324)

Who won 1st and 2nd Prizes and also a Cash Prize of Rs.10,000/-

In the Event Pushpak-ROBOVEDA'2021

AT SRINIDHI INSTITUTE OF SCIENCE AND TECHNOLOGY

Ghatkersar, Hyderabad



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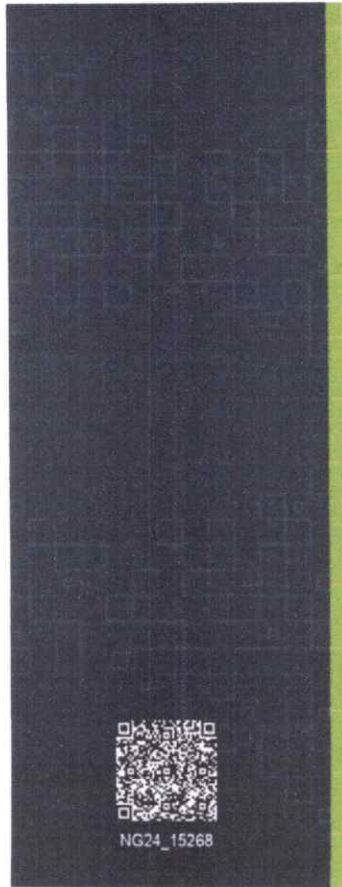
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5. Integrated tools: Students are encouraged to enroll in online courses



CERTIFICATE OF COMPLETION

This certificate is presented to

B Sanketh Kumar

for successful completion of the course on
Full Stack Application Development with Cloud Computing
under Next Gen Employability Program 2023-24.

Dr. Ramesh Unnikrishnan
Advisor T & L bureau
AICTE

Shrikant Sinha
Chief Executive Officer
TASK

Nagesh Singh
Executive Director
Edunet Foundation

Mr. B.SankethKumar,student of CSE Department has completed internship at EY(A.Y 2023-24)

Principal

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CERTIFICATE OF COMPLETION

This certificate is presented to

B Vaishnavi

for successful completion of the course on
Full Stack Application Development with Cloud Computing
under Next Gen Employability Program 2023-24.

Dr. Ramesh Unnikrishnan
Advisor T & L bureau
AICTE

Shrikant Sinha
Chief Executive Officer
TASK

Nagesh Singh
Executive Director
Edunet Foundation



NG24_15279

Miss B.Vaishnavi, student of CSE Department has completed internship at EY(A.Y 2023-24)

D. Praveen
Principal

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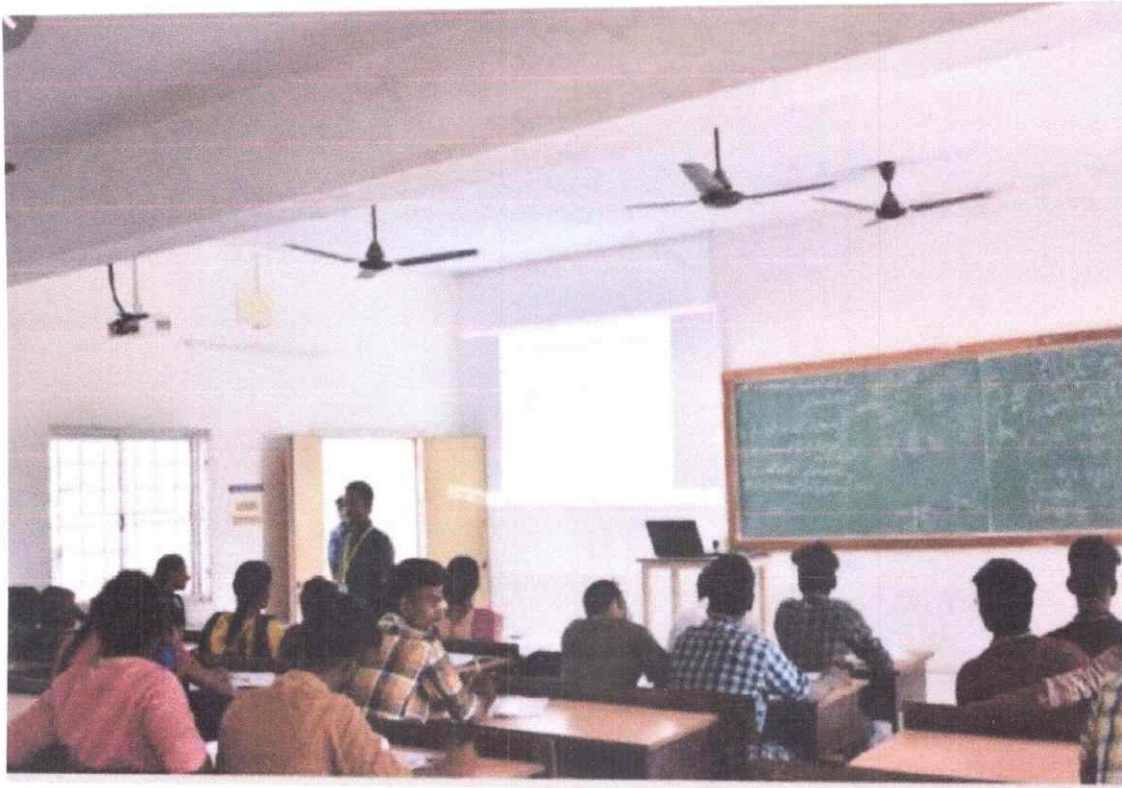
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6. Bridge course: conducted bridge course for the students filling the gaps in academic year courses



Students of III rd year II Semester participated in add on program “ **TOTAL STATION**” From 9-07-2023 to 20 -07-2023 delivered by DR. GURU PREM, Professor of civil department (A. Y 23-24)

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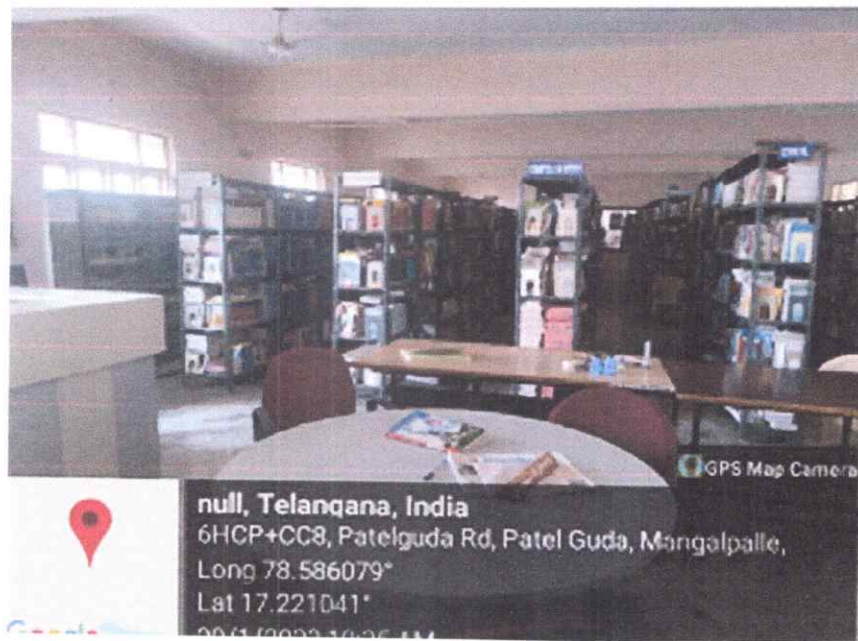
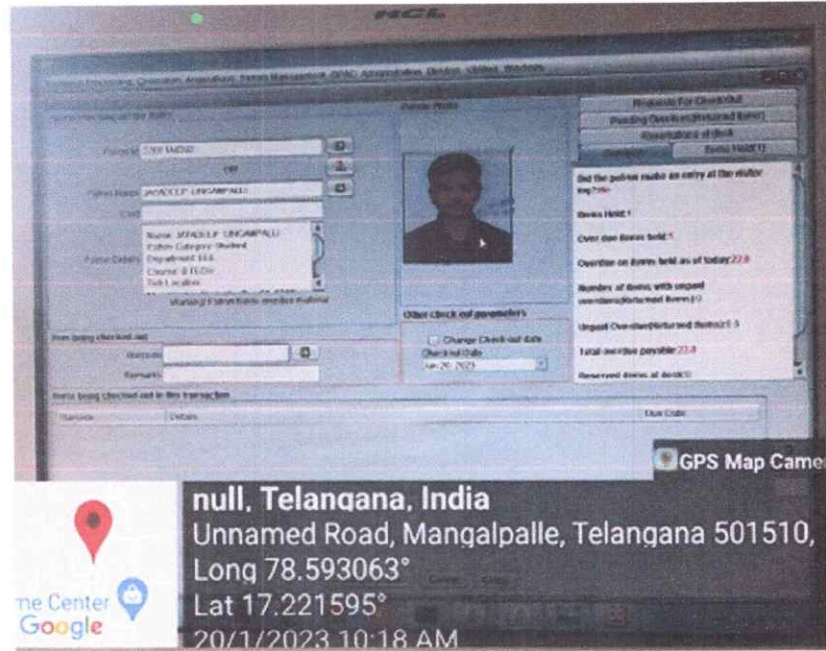
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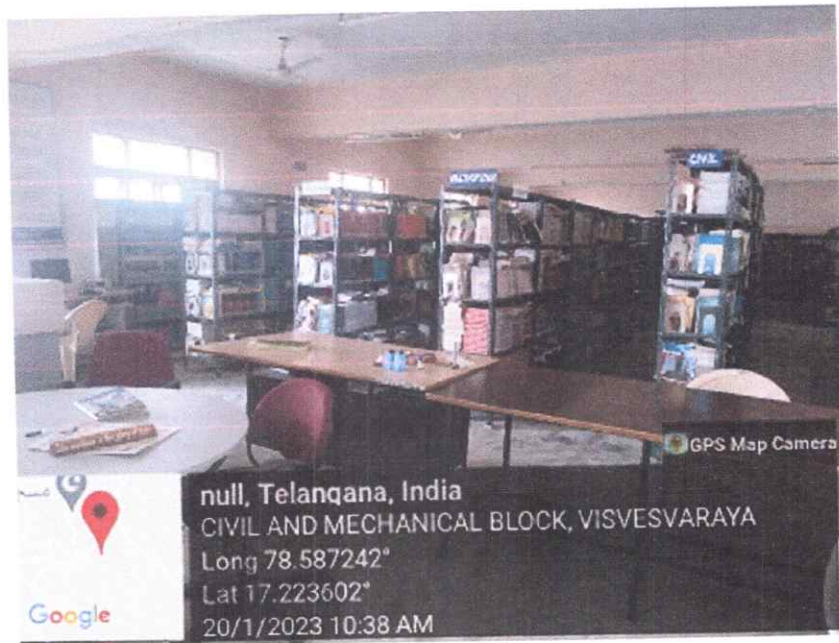
7. E-Learning: The institute allowed in access text books & references, course materials, Projects Reports , magazines, printed journals & E-journals.



M.P. Patel

Principal

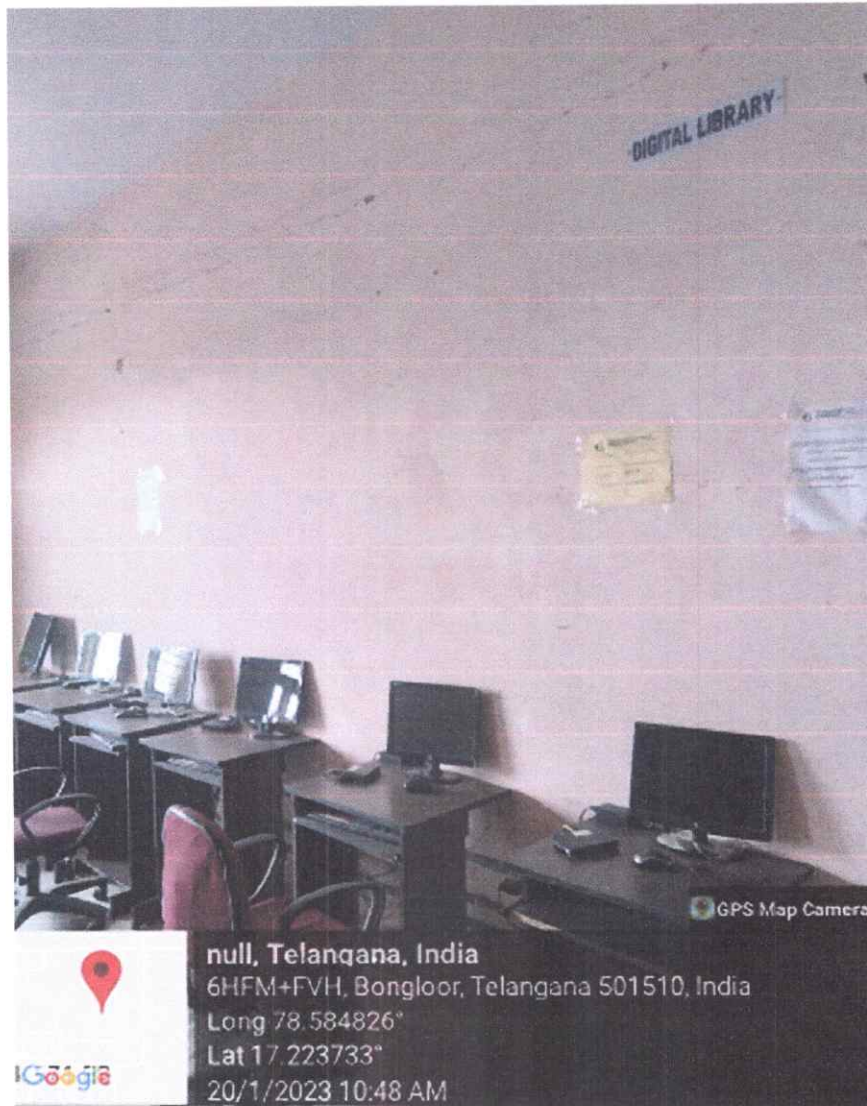
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D.P.

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D. Ravi

Principal

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8. Workshops, Guest lectures and Seminars: Students are encouraged to train on latest trends and innovative technologies by organizing workshops, guest lecturers and seminars



ARTS OF SMART WORK BT SRINIVASAN ON 07/01/2023

D. Paul
Principal

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EMBEDDED SYSTEMS 8051 MICROCONTROLLER BY RASAGNYA
FROM 24/11/2023 TO 26/11/2023



Programming Essentials in Python by Rakesh reddy



COMMUNICATION SKILLS BY MARK LOUIS

D. Praveen
Principal
Visvesvaraya College of Engineering & Technology
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9. Group Discussion & Debates: Encouraging students to participate in debates and discussions



D. Ram
Principal
Visvesvaraya College of Engineering & Technology
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Ranga Reddy (Dist), TS-501 519.



Organizational and interview skills by G.N.Satish on 9/01/2024 to 10/01/2024



Group Discussion

D.P.

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10. Technical Presentation: The students are encourage to participate in technical events to show case their presentation skills through poster, paper and model presentation and to contribute articles to the college magazines.

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ADVITIYA-2024
TECH FEST

TECHNICAL EVENTS :
PROJECT EXPO
TECHNICAL QUIZ
POSTER PRESENTATION
START-UP & BUSINESS IDEAS

CHIEF PATRONS :-
SRI.K.LAXMI NARAYANA GARU
SRI.A.SREEDHAR REDDY GARU
SRI.B.RAMULU GARU

PATRONS : DR.D.RAMESH PRINCIPAL
CONVENER : MR.V.HIRISH REDDY
@ advitiya_2k24

CULTURAL EVENTS :
FOOD STALLS
FLASH MOB
CULTURAL ACTIVITIES
(DANCE,SINGING,COMEDY)

STUDENT CO-ORDINATORS :
R.POOJITHA (CIVIL)
S.SAI TEJA (EEE)
G.MAHESH (MECH)
B.KIRAN (ECE)
J.SREEJA (CSE)
I.KARTHIK REDDY (CSM)

MAIL YOUR PAPERS TO :
advitiya24vcet@gmail.com
LAST DATE FOR SUBMISSION : 06-05-2024

MAY 7TH & 8TH

SCAN




D. P. ...

Principal

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Paper presentation on topic “CLOUD COMPUTING” by IV CSE Students from SREE VISVESVARAYA INSTITUTE OF TECHNOLOGY AND SCIENCE COLLEGE(A. Y 23-24)



Paper presentation on topic “ARITIFICIAL INTELLIGENCE” by III CSE Students from SIDDHARTHA INSTITUTE OF ENGINEERING AND TECHNOLOGY.(A. Y 23-24)

D. Ravi
Principal

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Paper presentation on topic “Computer Networks” by III CSE Students from VISVESVARAYA COLLEGE OF ENGINEERING AND TECHNOLOGY.

(A.Y 23-24)



Hand Art gallery by I1 AIML Students from VISVESVARAYA COLLEGE OF ENGINEERING AND TECHNOLOGY. (A.Y 23-24)

D. P. Ravi

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D. Ravi
Principal

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11. Alumni Interactions:

Alumni meets are organized every year to build the strong relationship between students and alumni to share their experience and knowledge towards career building.



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ALUMNI ENGAGEMENT MEETING event i.e., 27.07.2023.

D. Ramesh
Principal
Visvesvaraya College of Engineering & Technology
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Ranga Reddy (Dist), TS-501 510.



12. THINK-PAIR & SHARE: This module has been implemented to help students come out with their innovative or unique ideas where students work together to solve a problem or answer a question about an assigned reading.



Students of IV year II semester CSE discussing a technical topic in a class room
(Ac.Yr 2023-2024)



First year MBA students trying to share their ideas about management skills during a seminar held (Ac.Yr 2023-2024)

D. Ravi

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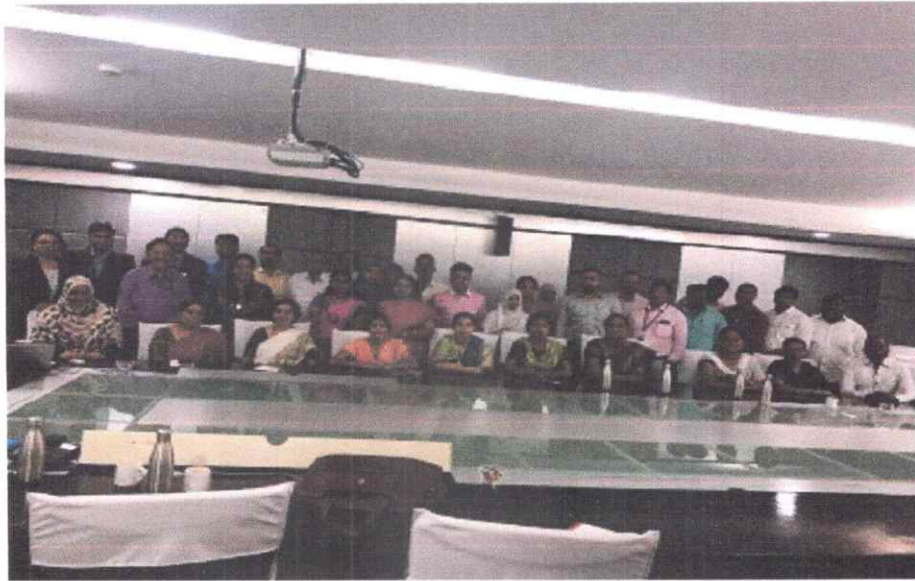
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13. Technical club activities: The institution has various professional societies like I EEE, IETE, IEL, CSI, SAE, ISIE, ISO, where the students actively participate in activities.



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Students and Faculty participated in various professional societies like IEEE, IETE, IEL, CSI, SAE, ISIE, ISO activities.

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14. Hands-on training programmes: in every year students undergo the training activities to explore in industry and advanced technologies



Students of AIML IInd year II Semester students, exhibiting Art gallery in VCET (A.Y 2023-24)

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15. Assignments & Quizzes: Used to analyse the performance and the understanding capability of each student at the end of the concept.

VISVESVARAYA COLLEGE OF ENGINEERING AND TECHNOLOGY Set-1
 MP Patelguda, Bongloor X Roads, Ibrahimpatnam, Ranga Reddy Dist, 501510, Telangana
 III B.Tech II semester (R-18 Regulation) (Academic year 2023-2024)
 I-Mid Term Examination May (2023)

Branch & Section: CSE Date of Exam: / / 2024
 Subject: Compiler Design Session & Time: 10:00 (FN) to 12:00 (FN)

NAME: Dreavathika Hall-Ticket No: 21071A0512

Part: A

I. Choose the correct alternative

S.NO	QUESTION	CORRECT CHOICE
	What is the purpose of a compiler?	
1	a) To convert source code into machine code b) To check the syntax of the source code c) To optimize the code for better performance d) To generate object code from assembly code	a
2	Which phase of the compiler is responsible for code generation?	d
	a) Lexical analysis b) Syntax analysis c) Semantic analysis d) Code generation	
3	What is the minimum number of MOV instructions in the code generated for a basic block if all operands are initially in memory and the final value of the computation is also in memory?	a
	a) 3 b) 2 c) 6 d) 4	
4	What is the purpose of the lexical analyzer in a compiler?	c
	a) To generate machine code b) To check the syntax of the source code c) To divide the source code into tokens d) To optimize the code for better performance	
5	What is the process of forming tokens from an input stream of characters called?	b
	a) Liberalization b) Tokenization c) Characterization d) None of the mentioned	
6	What is the purpose of syntax analysis in compiler design?	b
	a) To generate machine code b) To check the syntax of the source code c) To divide the source code into tokens d) To optimize the code for better performance	
7	Which type of parsing starts from the start symbol and tries to rewrite it to the input string?	a
	a) Top-down parsing b) Bottom-up parsing c) Left-to-right parsing d) Right-to-left parsing	
8	Which type of parsing is more powerful and can handle a larger class of grammars?	b
	a) LR parsing b) LR parsing c) LR parsing d) LR parsing	
9	Which phase of the compiler performs the syntax analysis?	c
	a) Lexical analysis b) Semantic analysis c) Syntax analysis d) Code generation	
10	What is the order of evaluation for synthesized attributes in syntax-directed translation?	b
	a) Pre-order traversal b) Post-order traversal c) In-order traversal d) Breadth-first traversal	

II. Fill in the blanks

1. The intermediate code generated by the compiler called Target code generation

2. Symbol table data structure is responsible for managing information about variables in a compiler

3. Lexical analysis phase of the compiler is responsible for recognizing tokens

4. What is the sequence of characters included in the source program according to the matching pattern of a token called lexeme

5. What is the main purpose of optimizing DFA-based pattern matchers in lexical analysis? to improve the pattern matching algo efficiency & performance

6. context-free grammar type of grammar is used in syntax analysis

7. LR(1) parsing type of parsing uses lookahead symbols to distinguish the grammar

8. What is the output of the syntax analysis phase in compiler design? an abstract syntax tree

9. Attributes associated with non-terminal definitions are used in syntax-directed translation

10. The order of evaluation for synthesized attributes in syntax-directed translation bottom up or post order, traversal of the parse tree

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Describe the routing information protocol and distance vector routing with an example?

A:- Routing information protocol (RIP):- It is a dynamic routing protocol that uses hop count as a routing metric to find the best path b/w source, and destination network.

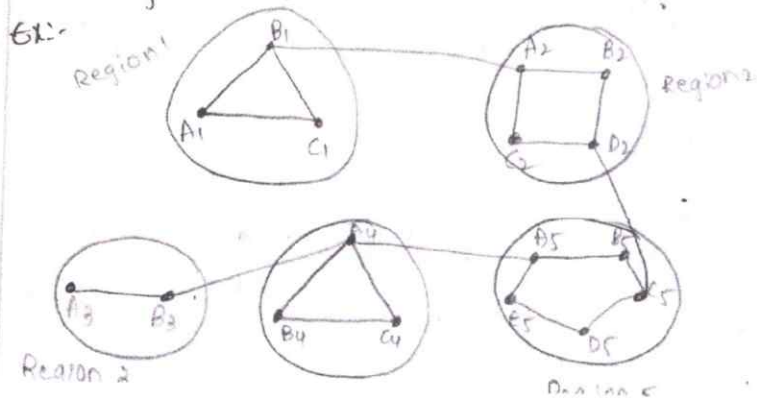
Hop count:- Hop count is the no. of routers occurring in b/w the source and destination network.

→ The path with the lowest hopcount is considered as the best route to reach a n/w & placed in the routing table.

→ The max. hop count allowed for RIP is 15 and hop count of 16 is considered as network unreachable.

Features of RIP:

1. Updates of the n/w are exchanged periodically.
2. Updates (routing information) are always broadcast.
3. Full routing tables are sent in updates.
4. Router always trust routing information received from neighbouring routers.



From A₁

Destination	Line	Hops
A ₁	-	-
B ₁	B ₁	1
C ₁	C ₁	1
A ₂	B ₁	2
B ₂	B ₁	3
C ₂	B ₁	3
D ₂	B ₁	C ₁
A ₃	C ₁	3
B ₃	C ₁	2
A ₄	C ₁	3
B ₄	C ₁	4
C ₄	C ₁	4
A ₅	C ₁	4
B ₅	C ₁	5
C ₅	B ₁	5
D ₅	B ₁ /C ₁	6
E ₅	C ₁	5

sharing information through Regions:

source destination line hops

R₁A₁ → R₂ → B₁ → A₂ - 2

R₁A₁ → R₃ → C₁ → B₃ - 2

R₁A₁ → R₄ → C₁ → A₄ - 3

R₁A₁ → R₅ → C₁ → A₅ - 4

Distance Vector Routing (DVR) protocol:- A DVR protocol requires that a router inform its neighbours of topology changes periodically. Historically known as old ARPANET routing algorithm (or) Bellman-ford Algorithm.

Bellman-ford Basics:- Each router maintains a distance vector table containing the distance b/w itself & all possible destination nodes. Distance based on a chosen metric, are computed using information from neighbour's distance vectors -

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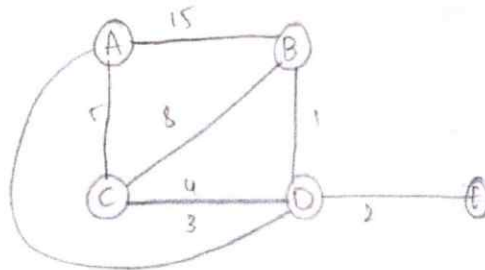
- Each router has an ID
- Associated with each link connected to a router, there is a link cost (static or dynamic)
- Intermediate hops
- Distance Vector table initialization:-
 - * Distance to itself = 0
 - * Distance to all other routers = infinity number

Distance Vector Algorithm:-

1. A router transmits its distance vector to each of its neighbour in a routing protocol.
 2. Each router receives & saves the most recently received distance vector from each of its neighbours.
 3. A router recalculates its distance vector
- The DV calculation is based on minimizing the cost to each destination.

$$d_x(y) = \{ c(x,u) + d_u(y) \}$$

Ex:-



D. Ramesh

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Destination	cost	NextHop
A	0	-
B	15	B
C	5	C
D	3	D
E	∞/5	D

From B

Destination	cost	NextHop
A	15	A
B	0	-
C	8	C
D	1	D
E	∞/3	D

From C

Destination	cost	NextHop
A	5	A
B	8	B
C	0	-
D	4	D
E	∞/6	D

From D

Destination	cost	NextHop
A	B	A
B	1	B
C	4	C
D	0	-
E	2	E

From E

Destination	cost	NextHop
A	∞/5	D
B	∞/3	D
C	∞/3	D
D	2	D
E	0	-

$$\rightarrow d(x,y) = (c(x,v) + d(v,y)) \}$$

From A to E:-

$$\begin{aligned}
 d_A(E) &= \{ c(A,B) + (B,D) + (D,E) \\
 &\Rightarrow c(A,C) + (C,D) + (D,E), \\
 &\quad c(A,D) + (D,E) \} \\
 &= \{ 15 + 1 + 2, 5 + 4 + 2, 3 + 2 \} \\
 &= \{ 8, 11, 5 \}
 \end{aligned}$$

D. P. Rao

Principal



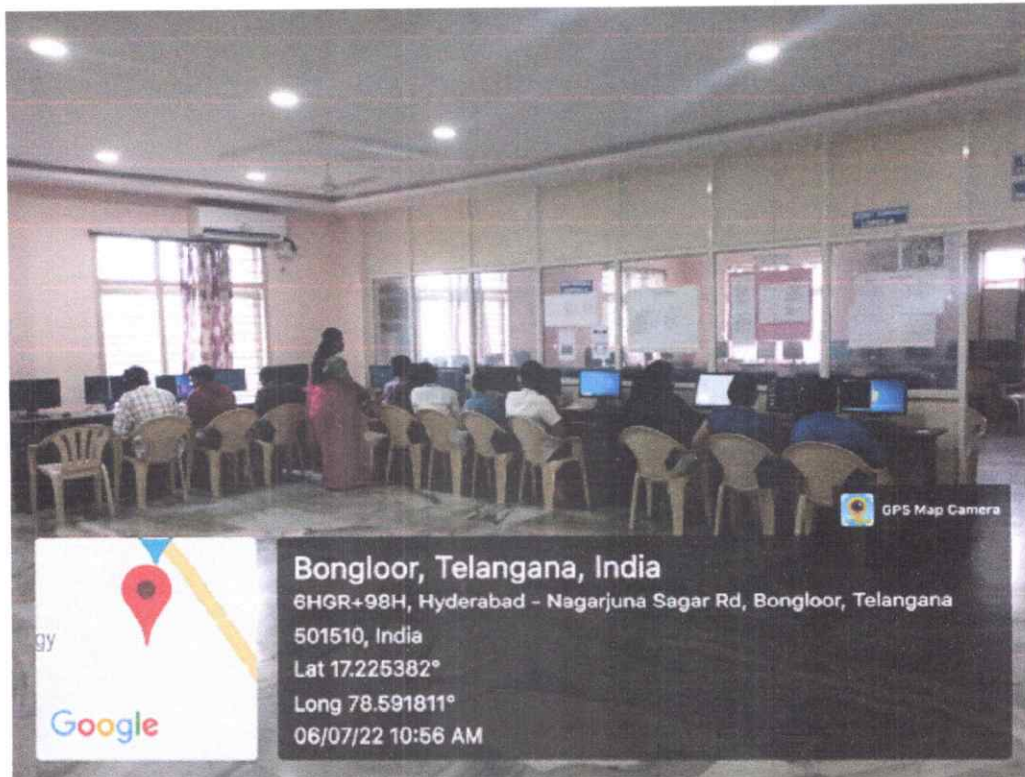
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16. Virtual labs: Used to provide remote-access to Labs in various disciplines can avail the various tools for learning, including additional web-resources, video-lectures, animated demonstrations and self-evaluation.



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